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(54) Intermediate trigger voltage ESD protection device

(57) The present invention is related to a semiconductor device for electrostatic discharge or overvoltage protection applications, said device comprising means for absorbing an electrostatic discharge pulse or an overvoltage level, said means being triggered at intermediate voltages and said means including a series configuration of at least two trigger components (551,542). Said means can further be extended with a third trigger component (8024) and possibly further trigger components in said series configuration, the addition of said third and further trigger components extending sequentially the range of the intermediate trigger voltages. Said trigger components can comprise components, preferably diodes, with a specific breakdown voltage, the sum of the breakdwon voltages of said diodes defining the specific intermediate trigger voltage of said device.

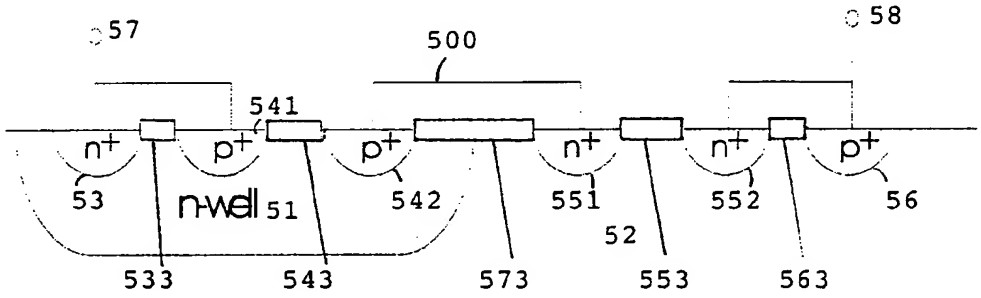

FIG. 5a

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Description

Field of the invention

[0001] The present invention is related to a semiconductor device and a circuit for electrostatic discharge and overvoltage protection applications.

Background of the invention

[0002] Electronic devices and circuits are to be protected against damage arising from electrostatic discharge pulses, current transients or overvoltage levels. Protection devices or circuits using silicon controlled rectifier structures (SCR) are known in the art. SCR devices were applied frequently as an efficient electrostatic discharge protection clamp. These devices are made such that as a result of electrostatic discharge (ESD) pulses, current transients or overvoltage levels, an n-p-n-p thyristor structure is triggered whereby ensuring the clamping of the ESD-pulses, and snapback of the device to very low holding voltages. These devices furthermore are such that this absorption of electrostatic discharge pulses, current transients or overvoltage levels leads to low power dissipation after triggering. Examples of such SCR devices are disclosed in the patents US-5072273, US-5343053 and US-5663860.

[0003] A cross-section of a prior art classical SCR-device is shown on Figure 1. The SCR-device is fabricated in a semiconductor substrate (12) of a p-type conductivity with a n-well (11) therein. In the figure, the pad connection (17) is connected to both the n-well contact region (13) and a p+-region (14) inside the n-well. The ground is connected to the p-substrate contact region (16) and an n+-region (15) inside the p-substrate (12). An equivalent circuit schematic is shown on Fig. 2. It comprises a parasitic pnp (299) and a parasitic npn transistor (200) that are connected. The npn-transistor (200) consist of the n-well/p-substrate/n+ region, whereas the pnp-transistor (299) consists of the p+-region/n-well/p-substrate.

[0004] In normal operating conditions, the SCR-device is off. When a positive ESD-pulse is applied at the pad, the n-well (11) to p-substrate (12) diode (11)/(12) is reverse biased, until it goes into breakdown. This typically happens at voltages in the order of 40-50V. Once the n-well/substrate diode is in breakdown, electron-hole pairs are generated in the space-charge region of this diode. The holes are flowing to the p-substrate contact (16), whereas the electrons are flowing to the n-well contact (13). Due to the substrate resistance Rsub, the p-base of the parasitic npn transistor (200) is charging up, and when the base voltage is becoming higher than 0.7V, this npn parasitic transistor is triggered. At about the same time the pnp transistor is triggered due to the charging up phenomenon, and via a positive feedback mechanism, the device is latched into a low impedant state, with a low holding voltage of typically 2-3 Volt, or in some applications 3-4V, and a low series resistance of typical a few Ohm, which leads to very low power dissipation and high ESD-thresholds.

[0005] The problem of most of the classical SCR devices is that the trigger voltage at which the device goes into the low-impedant on-state is quite high, typically 50V, which is too high for normal low-voltage technologies. In order to allow the use of SCR-devices, but avoid the high trigger voltages, a so-called low-voltage triggered SCR (LVTSCR) has been proposed. A cross section of the LVTSCR is shown on Fig. 3, and an equivalent circuit schematic is shown on Fig. 4. In this protection device, an n+region (39) is implanted at the edge between the n-well (31) and the p-substrate (32). The n+-region/p-substrate junction will go into breakdown at a lower voltage, typical 13-14V, in this way lowering the triggering voltage of the SCR. The n+-region can be separated from the n+region in the p-substrate either by a field oxide or by a poly-gate (395, shown in figure 3). In the latter case, the gate of the parasitic nMOS is connected to the ground, as is shown on Fig. 3 and 4. This device is well suited to protect technologies with normal operating voltages.

Aims of the invention

[0006] The classical SCR protection devices are typically suited for high voltage applications, whereas the LVTSCR structure is frequently used for normal operating voltage applications. For some applications, however, the low trigger voltage (for instance of 14V) for an LVTSCR is too low, whereas the high trigger voltage (for instance of 50V) for the classical SCR is too high. As a result, there is a need for SCR-structures that trigger at intermediate voltages, or for which the trigger voltage can be adapted, depending on the application.

[0007] The present invention aims to fill this gap in protection devices. The present invention aims to disclose a semiconductor device for electrostatic discharge or overvoltage protection applications, said device comprising means for absorbing an electrostatic discharge pulse or an overvoltage level, said means being triggered at intermediate voltages.

[0008] The present invention furthermore aims to disclose a semiconductor device for electrostatic discharge or overvoltage protection applications, said device comprising means for absorbing an electrostatic discharge pulse or an overvoltage level, said means being triggered at intermediate voltages and said means being extendable with a third trigger component and possibly further trigger components, the addition of said third and further trigger components extending sequentially the range of the intermediate trigger voltages such that the protection trigger voltage can be adapted depending on the application.

Summary of the invention

[0009] In a first aspect of the present invention, a semiconductor device for electrostatic discharge or overvoltage protection applications is disclosed, said device comprising means for absorbing an electrostatic discharge pulse or an overvoltage level, said means being triggered at intermediate voltages and said means including a series configuration of at least two trigger components. Said means can further be extended with a third trigger component and possibly further trigger components in said series configuration, the addition of said third and further trigger components extending sequentially the range of the intermediate trigger voltages. Said trigger components can comprise components, preferably diodes, with a specific breakdown voltage, the sum of the breakdown voltages of said diodes defining the specific intermediate trigger voltage of said device.

[0010] In another embodiment of the device of the invention according to the first aspect, the device can further comprise an integrated circuit having a functionality and an impedance being in the connection of said means to said circuit. The impedance can be replaced by any means being adapted for building up a voltage drop. The impedance preferably is a resistor. Said circuit further comprises components or has components in parallel or connected to the circuit, components that convert an overvoltage level or an electrostatic discharge pulse of an intermediate level into an electrical current, said current creating a voltage of an intermediate level over said impedance, said voltage triggering said means such that said overvoltage level or electrostatic discharge pulse is absorbed.

[0011] For the purpose of this patent application, the following terms are introduced here. A trigger component, or triggering component, has the meaning that in the devices of the invention, at least one component or the triggering component is made such that as a result of electrostatic discharge (ESD) pulses, current transients or overvoltage levels, this component is triggered whereby ensuring the clamping of the ESD-pulses, and snapback of the device to very low holding voltages. Thus the electrostatic discharge pulses, current transients or overvoltage levels are absorbed in the device of the invention by making use of the above-introduced trigger components and further in such a way that a low power dissipation occurs in the device after triggering and snapback of the device to the low holding voltages. Low, high and intermediate voltages are to be understood in the context of a specific protection application for a specific technology. The terms low, high and intermediate voltage levels refer to overvoltage levels or to voltage levels resulting from electrostatic discharge pulses. Such voltages are higher than the normal operating voltages of electronic systems and can be classified in terms of high, intermediate and low overvoltage levels, the specific voltage values corresponding to high, low and intermediate being dependent on the specific technology. For the mainstream applications as for instance a 0.7 µm CMOS technology, the normal operating voltages are of the order of 5-12 Volt. A high overvoltage level is than referred to as about 40-50 Volt. A low overvoltage level is referred to as of the order of 14 Volt. Intermediate voltage levels are levels therebetween. Thus, the specific values of the terms low, high and intermediate voltage levels depend on the specific application, specifically on the values of the normal operating voltages of the specific technology. It is known in the art that the normal operating voltages for instance a 0.25 µm CMOS technology are lower than 5-12 Volt. Thus the value of a low overvoltage level may also be lower than 14 Volt and the value of a high overvoltage level may also be lower than or equal to, or even be higher than 50 Volt.

[0012] In a second aspect of the present invention, a semiconductor device for electrostatic discharge or overvoltage protection applications is disclosed, said device comprising a first region of a first conductivity type in a semiconducting substrate of a second conductivity type and at least two separated regions of said second conductivity type being within said first region, said separated regions of said second conductivity type not abutting the substrate region of said second conductivity type. The device further comprises at least two separated regions of said first conductivity type being within said substrate, said separated regions of said first conductivity type not abutting said first region; and a connection inbetween at least one of said separated regions of said second conductivity type within said first region and at least one of said separated regions of said first conductivity type within said substrate.

[0013] The connection is such that said device is absorbing an electrostatic discharge pulse or an overvoltage level at an intermediate voltage level. In a first embodiment of this second aspect of the invention, said connection can be a low-resistive connection, preferably a metal line, and preferably external to said first region and to said substrate. In a second embodiment, said connection can comprise at least one component having a breakdown voltage, said component being in series with said separated regions of said second conductivity type and said separated regions of said first conductivity type. According to this second embodiment of the invention said connection can comprise at least one region of said first and/or at least one region of said second conductivity type, said regions being within a second region of either one of said conductivity types, the second region being of the other (second or first) conductivity type than the embedded region (of a first or second conductivity type resp.). One of these regions in the second region can be present as a contact region. Additional regions can be embedded within said second region. Preferably this second region is within said substrate and is of said first conductivity type. At least part of the regions that are embedded within said second region are connected to the separated regions in the first

region and in the substrate. Specifically, one region of said first conductivity (one region of these embedded regions in the second region) can be directly connected with a low-resistive connection to one of the separated regions of said second conductivity type in the first region. Furthermore, one region of said second conductivity type of these embedded regions can be directly connected with a low-resistive connection to one of the separated regions of said first conductivity type in said substrate.

[0014] In the device of the invention, the regions of at least one of the set of said separated regions can be separated by an insulating material, said material preferably comprising an oxide material. The separated regions can also be separated by a control terminal overlying said substrate or said first region with an insulating material therebetween. One region of at least one of the set of said separated regions can be directly connected to the control terminal of said one set.

[0015] In the device of the invention according to the second aspect of the invention, said first region of said first conductivity type can be connected to a pad contact and said substrate of said second conductivity type is connected to ground, the connections to said pad contact and to ground preferably being via a highly doped contact region in said first region and said substrate respectively. It is evident that the reverse configuration can be made as well: said first region of said first conductivity type being connected to ground and said substrate of said second conductivity type being connected to a pad contact. A pad contact is the bonding pad connection of the device to the external devices or structures. Preferably, it is an Input/Output pad, or the connection to the package of the device, or the connection to the programming pin for fuses, or the connection to the supply voltage.

[0016] In an embodiment of the invention, the device of the invention can be integrated within said substrate with an integrated circuit having a functionality and that needs to be protected against overvoltage levels or electrostatic discharge pulses. The connection to such integrated circuit can also be done via the bonding pad.

[0017] In a third aspect of the invention, a protection circuit for electrostatic discharge or overvoltage protection applications is disclosed, said circuit comprising at least two, preferably MOS, transistors in series, said transistors having at least two electrodes and one control terminal, one electrode of the first transistor being connected to one electrode of the second transistor, the other electrode of said transistors being connected to the respective control terminals of said transistors. Said transistors preferably are of the opposite type and one control terminal of one transistor can be grounded while the control terminal of the second transistor is connected to a pad contact.

[0018] In another embodiment of this third aspect of the invention, one electrode of the first transistor is directly connected to the one electrode of the second transistor. An additional junction of first and second conductivity type regions can be present inbetween the one electrode of the first transistor and the one electrode of the second transistor.

[0019] Yet all combinations of the different embodiments according to different aspects of the invention are feasible.

Short description of the drawings

[0020] Figure 1 shows the cross section of a prior art SCR-device.

[0021] Figure 2 shows an equivalent circuit representation of the SCR-device shown in figure 1.

[0022] Figure 3 shows the cross section of a prior art SCR-device with means for protection against low voltage pulses.

[0023] Figure 4 shows an equivalent circuit representation of the SCR-device shown in figure 3.

[0024] Figure 5a and 5b show the cross sections of embodiments of device of the invention.

[0025] Figure 6 shows the equivalent circuit representation of the SCR-devices shown in figure 5.

[0026] Figure 7 shows a characteristic of the device of the invention as shown in figure 5; the characteristic is measured with a TLP measurement set-up.

[0027] Figure 8 shows the cross section of another embodiment of the device of the invention.

[0028] Figure 9 shows the equivalent circuit representation of the SCR-device shown in figure 8.

[0029] Figure 10 shows a characteristic of the device of the invention as shown in figure 8; the characteristic is measured with a TLP measurement set-up.

[0030] Figure 11 shows the schematic representation of yet another embodiment of the invention.

Detailed description of the invention

[0031] For the purpose of teaching of the invention, several embodiments of the invention are disclosed in the sequel. In a best mode of the invention, the devices of the invention are fabricated in a 0.7 μm CMOS technology, the I2T technology offered by ALCATEL MICROELECTRONICS. The measurement characteristics shown in figure 7 and in figure 10 are taken on such devices. The design rules of this technology are known and the fabrication of the devices of the invention can be made making use of standard process steps being offered with this technology. It is evident that the person of skill in the art will be able to imagine other embodiments of the invention, the spirit and scope of the invention being limited only by the terms of the appended claims.

[0032] Cross sections of two embodiments of the devices of the invention are shown on Fig. 5, whereas two circuit equivalents are given in Fig. 6.

[0033] The semiconductor device of figure 5 is a device for electrostatic discharge or overvoltage protection

applications. The device comprises a first region (51) of a first conductivity type in a semiconducting substrate (52) of a second conductivity type and at least two separated regions (541) (542) of said second conductivity type being within said first region (51), said separated regions of said second conductivity type not abutting the substrate region of said second conductivity type. The device further comprises at least two separated regions of said first conductivity type (551) (552) being within said substrate, said separated regions of said first conductivity type not abutting said first region; and a connection (500) inbetween at least one of said separated regions of said second conductivity type within said first region and at least one of said separated regions of said first conductivity type within said substrate.

[0034] The connection is such that said device can absorb an electrostatic discharge pulse or an overvoltage level at an intermediate voltage level. Said connection according to the embodiment shown in figure 5a is a low-resistive connection, preferably a metal line (500), and preferably external to said first region and to said substrate.

[0035] In the device of the invention, the regions of at least one of the set of said separated regions can be separated by an insulating material, said material preferably comprising an oxide material (543) (553) (figure 5a). The separated regions can also be separated by a control terminal (505) overlying said substrate or said first region with an insulating material therebetween (figure 5b). Thus, a transistor configuration is formed among the sets of separated regions. One region of one or both sets of said separated regions can be directly connected to the control terminal of each set respectively.

[0036] In the device of the invention shown in figure 5, said first region of said first conductivity type is connected to a pad contact (57) and said semiconducting substrate of said second conductivity type is connected to ground (58), the connections to said paid contact and to ground preferably being via a highly doped contact region in said first region and said substrate respectively (53) (56). There are oxide regions (533) (543) (563) (573) inbetween the highly doped contact (53) (56) regions and the separated regions (541) (552) and inbetween the different separated regions (551) (542) referred to above.

[0037] In the device of the invention according to the embodiment shown in figure 5, two p^+ regions (541) (542) are implanted in a n-well (51), whereas two n^+ regions (551) (552) are implanted in the p-substrate (52). The implanted regions are separated and can have a spacing. This spacing is a design rule of the device and this spacing is of influence on the trigger voltage and snapback of the device. One region of each set of separated regions is connected to a region of the other set of separated regions (542)-(551), by a metal connection (500). The 2 p^+-regions (541) (542) in the n-well as well as the 2 n^+-regions (551) (552) in the substrate can be spaced apart by either a field oxide (LOCOS) or a polysilicon gate (a transistor structure). The former case is shown in Fig. 5a, whereas the latter case is shown in Figure 5b.

[0038] In the first equivalent circuit shown on Fig. 6, the structure is represented as a SCR merged transistor pair, with however a second collector for both the pnp and npn transistors. Both second collectors are connected to each other. In a second equivalent circuit scheme, the structure can be represented as being a series circuitry of a p-MOS and an n-MOS transistor, with the source and the gate of the p-MOS connected to the pad, and the source and the gate of the n-MOS connected to the ground, whereas the drains of both nMOS and pMOS are connected to each other.

[0039] The operation of the new device is as follows. When a positive ESD pulse is applied to the pad, the structure is initially off, as both p-MOS and n-MOS transistors (600) (699) as well as both parasitic bipolar transistors are off. The device will go into breakdown when either the n-well to substrate junction breaks down, which happens at 40-50V, or when both the second p^+/n-well diode (542)/(51) and the second $n+$/p-substrate diode (551)/(52), which are connected in series, are going into breakdown, i.e. when the drain of both the nMOS and the pMOS transistor are going into breakdown. The latter happens typically at a voltage equal to the sum of both breakdown voltages:

$$V_{BD} = V_{BDn+p} + V_{BDn+p}$$

which is typically 26-28V, and therefore the n-well/p-substrate will not trigger first. The electron/hole pairs generated in both the drains of the nMOS and pMOS transistors will flow to the $n+$-well and p-substrate contacts, respectively, and will eventually trigger the nMOS and/or pMOS transistor into snapback. This then triggers the complete SCR into the low holding voltage state. This means that this SCR-structure has a trigger voltage of 26-28V, but still shows a low holding voltage of the device.

[0040] Measurement characteristics on devices according to the embodiment shown in figure 5/6 are shown in figure 7. The measurement characteristic is taken with a Transmission Line Pulse (TLP) set-up which is a measurement technique that is known in the art. The TLP set-up creates a voltage/current pulse over the device of the invention and the response is recorded. It is seen from the characteristic in figure 7 that the device of the invention has a trigger voltage (V_{snap}) of about 26 Volt at which stage the device goes into snapback and the device can withstand a current of higher than 1,5 A at the low holding voltages shown in the figure.

[0041] In another embodiment of the device, an additional diode (901), a component with a breakdown voltage, or more diodes can be inserted between the two

drains of the nMOS and pMOS (i.e. between the two extra collectors of the parasitic npn and pnp transistors). This embodiment of the invention is shown in figure 8. A second n-well (802) is made in the p-type substrate in addition to the first n-well region (801). A n^+ region and a p^+ region are implanted in the second n-well. The n^+ region is serving as contact region. The p^+ region (8024) is forming a diode with the n-well. This diode can thus be constructed as a p^+/n-well diode, where the p^+ region is connected to the drain of the nMOS (851), and the n-well is connected to the drain of the pMOS (842). A schematic of this variation is shown on Fig. 9. This structure operates in substantially the same way as the previous embodiment shown in figure 5, except that it will trigger at a voltage equal to

$$V_{BD} = V_{BDn+p} + 2\,V_{BDp+n}$$

which is typically 38-42V.

[0042] Measurement characteristics on devices according to the embodiment shown in figure 8/9 are shown in figure 10. The measurement characteristic is taken with a Transmission Line Pulse (TLP) set-up which is a measurement technique that is known in the art. The TLP set-up creates a voltage/current pulse over the device of the invention and the response is recorded. It is seen from the characteristic in figure 10 that the device of the invention has a trigger voltage (V_{snap}) of about 38 Volt at which stage the device goes into snap-back and the device can withstand a current of higher than 4 A at the low holding voltages shown in the figure.

[0043] It is shown with the present embodiments that the trigger voltage gap between 13-14V and 50V can be filled with new SCR structures that are triggering at intermediate voltages of 26-28V and 38-42V. Thus, these embodiments show a device for electrostatic discharge or overvoltage protection applications. A semiconductor device for electrostatic discharge or overvoltage protection applications is disclosed, said device comprising means for absorbing an electrostatic discharge pulse or an overvoltage level, said means being triggered at intermediate voltages and said means being in a series configuration of at least two trigger components (542)/(51), (842)/(81) and (551)/(52), (851)/(82). Said means can further be extended with a third trigger component (901) and possibly further trigger components in said series configuration, the addition of said third and further trigger components extending sequentially the range of the intermediate trigger voltages.

[0044] Yet in another embodiment of the invention, the schematic of which is shown in figure 11, the device can further comprise an integrated circuit having a functionality and an impedance (1101) being in the connection of said means (110) to said circuit (1100). Said means and said circuit can be in a parallel configuration. The impedance can be replaced by any means being adapted for building up a voltage drop. The impedance preferably is a resistor as shown in figure 11. Typically the resistor has a value of about 100-500 Ω. Said circuit further comprises components or has components in parallel or connected to the circuit, components that convert an overvoltage level or an electrostatic discharge pulse of an intermediate level into an electrical current. These components can be two diodes in a series configuration that as a consequence thereof break down at an intermediate voltage level thereby creating said current in said resistor. Said current creates a voltage of an intermediate level over said impedance, said voltage triggering said means (110) such that said overvoltage level or electrostatic discharge pulse is absorbed in said means. The series configuration of the two diodes that go into breakdown is not adapted for absorbing the overvoltage level or electrostatic discharge pulse and therefore the means (110) of the device of the invention is needed. This embodiment of the device of the present invention is especially advantageous for taking up an overvoltage level or electrostatic discharge pulse during the first nanoseconds, about 1-3 ns, after the pulse or overvoltage level is applied to the circuit.

Claims

1. A semiconductor device for electrostatic discharge or overvoltage protection applications, said device comprising :
   - a first region of a first conductivity type in a semiconducting substrate of a second conductivity type, at least two separated regions of said second conductivity type being within said first region, said separated regions of said second conductivity type not abutting the substrate region of said second conductivity type ;
   - at least two separated regions of said first conductivity type being within said substrate, said separated regions of said first conductivity type not abutting said first region ; and
   - a connection being inbetween at least one of said separated regions of said second conductivity type within said first region and at least one of said separated regions of said first conductivity type within said substrate.

2. The device as recited in claim 1 wherein said connection is such that said device is adapted for absorbing an electrostatic discharge pulse or an overvoltage level of an intermediate voltage level.

3. The device as recited in claim 1 wherein said connection is a low-resistive connection preferably a metal line, and preferably external to said first region and to said substrate.

4. The device as recited in claim 1 wherein said connection comprises at least one component having a breakdown voltage, said component being in series with said separated regions of said second conductivity type and said separated regions of said first conductivity type.

5. The device as recited in claim 1 wherein said connection comprises at least one region of one (first or second) conductivity type, said region being within a second region of the other (second or first) of said conductivity types, said one region of said one conductivity being directly connected with a low-resistive connection to one of the separated regions of the other conductivity type.

6. The device as recited in any one of the preceding claims wherein said first and said second conductivity types are opposite conductivity types.

7. The device as recited in claim 1 wherein the regions of at least one of the set of said separated regions are separated by an insulating material, said material preferably comprising an oxide material.

8. The device as recited in claim 1 wherein the regions of at least one of the set of said separated regions are separated by a control terminal overlying said substrate or said first region with an insulating material therebetween.

9. The device as recited in claim 8 wherein one region of at least one of the set of said separated regions is directly connected to the control terminal of said one set.

10. The device as recited in claim 1 wherein said first region of said first conductivity type is connected to a pad contact and wherein said semiconducting substrate of said second conductivity type is connected to ground, the connections to said pad contact and to ground preferably being via a highly doped contact region in said first region and said substrate respectively.

11. The device as recited in claim 1 wherein the sets of separated regions are within the surface layer of respectively said first region and said substrate and wherein said device is made in a CMOS technology.

12. The device as recited in claim 11 being integrated within said substrate with an integrated circuit having a functionality.

13. A semiconductor device for electrostatic discharge or overvoltage protection applications, said device comprising means for absorbing an electrostatic discharge pulse or an overvoltage level, said means being triggered at intermediate voltages and said means including a series configuration of at least two trigger components.

14. The semiconductor device as recited in claim 13 wherein said means are extended with a third trigger component and possibly further trigger components in said series configuration, the addition of said third and further trigger components extending sequentially the range of the intermediate trigger voltages.

15. The semiconductor device as recited in claim 14 wherein said trigger components comprise components, preferably diodes, with a specific breakdown voltage, the sum of the breakdown voltages of said diodes defining the specific intermediate trigger voltage of said device.

16. The semiconductor device as recited in claim 13 further comprising an integrated circuit having a functionality and an impedance being in the connection of said means to said circuit, said circuit comprising components that convert an overvoltage level or an electrostatic discharge pulse of an intermediate level into an electrical current, said current creating a voltage over said impedance, said voltage triggering said means.

17. A protection circuit for electrostatic discharge or overvoltage protection applications, said circuit comprising at least two transistors in series, said transistors having at least two electrodes and one control terminal, one electrode of the first transistor being connected to one electrode of the second transistor, the other electrode of said transistors being connected to the respective control terminals of said transistors.

18. The circuit as recited in claim 17 wherein said transistors are of the opposite type.

19. The protection circuit as recited in claim 17 wherein the control terminal of one terminal is grounded and wherein the control terminal of the second transistor is connected to a pad contact.

20. The protection circuit as recited in claim 17 wherein the one electrode of the first transistor is directly connected to the one electrode of the second transistor.

21. The protection circuit as recited in claim 17 wherein an additional junction of first and second conductivity type regions is present inbetween the one electrode of the first transistor and the one electrode of the second transistor.

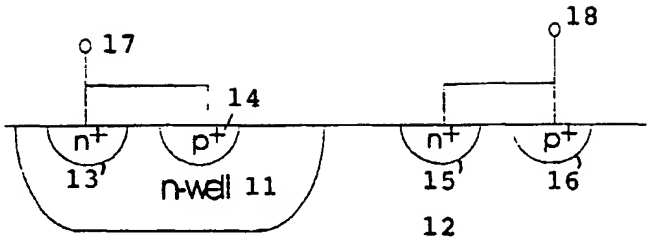
17
18
14
n+
p+
n+
p+
13
n-well 11
15
16
12

FIG. 1

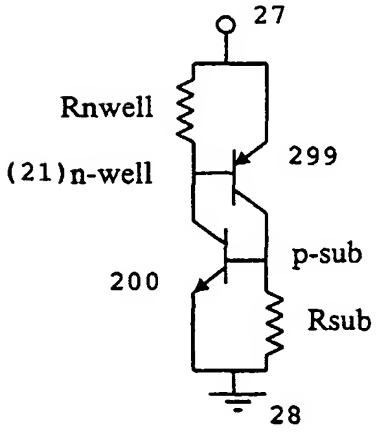
27
Rnwell
(21)n-well
299
p-sub
200
Rsub
28

FIG. 2

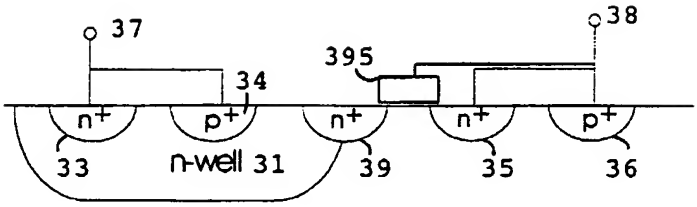
37
38
395
34
n+
p+
n+
n+
p+
33
n-well 31
39
35
36

FIG. 3

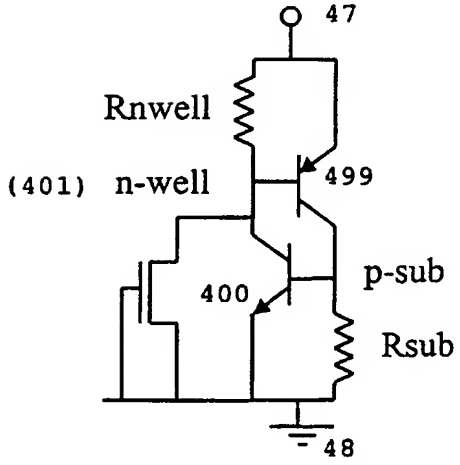
47
Rnwell
(401) n-well
499
p-sub
400
Rsub
48

FIG. 4

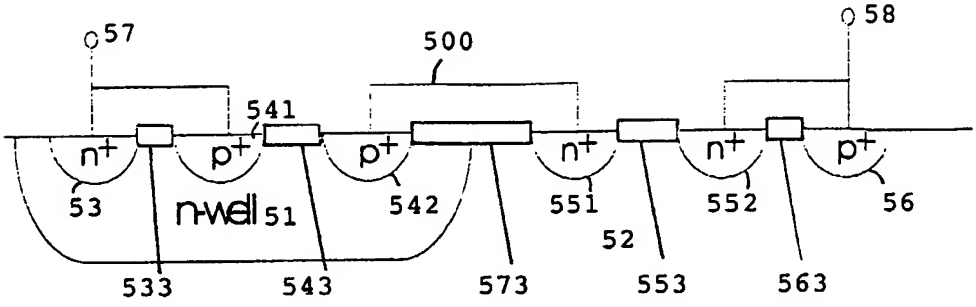
57
500
58
541
n+
p+
p+
n+
n+
p+
53
n-well 51
542
551
552
56
52
533
543
573
553
563

FIG. 5a

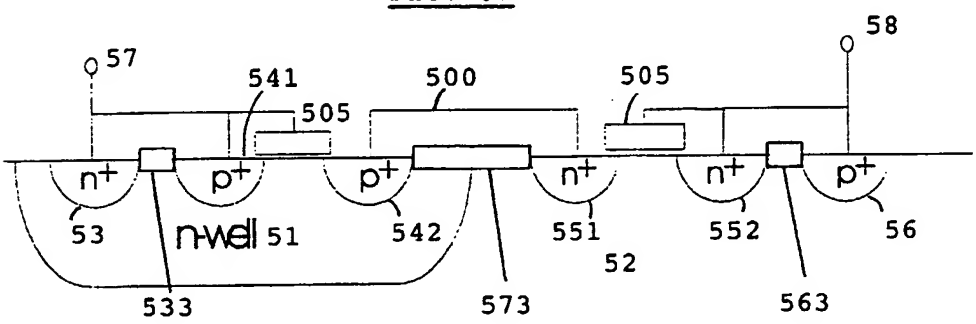
58
57
541
500
505
505
n+
p+
p+
n+
n+
p+
53
n-well 51
542
551
552
56
52
533
573
563

FIG. 5b

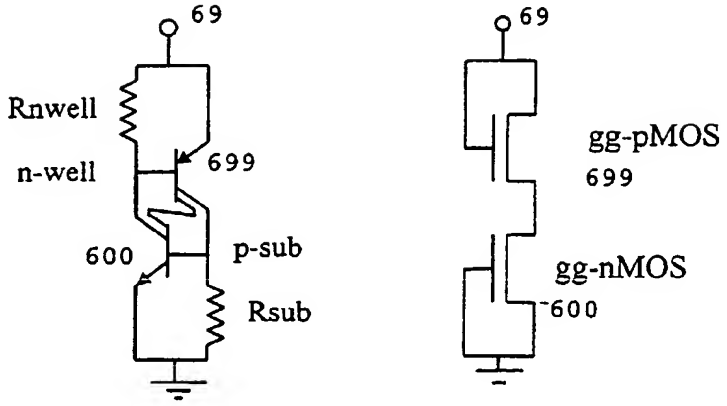
69
Rnwell
n-well
699
600
p-sub
Rsub
69
gg-pMOS
699
gg-nMOS
600

FIG. 6

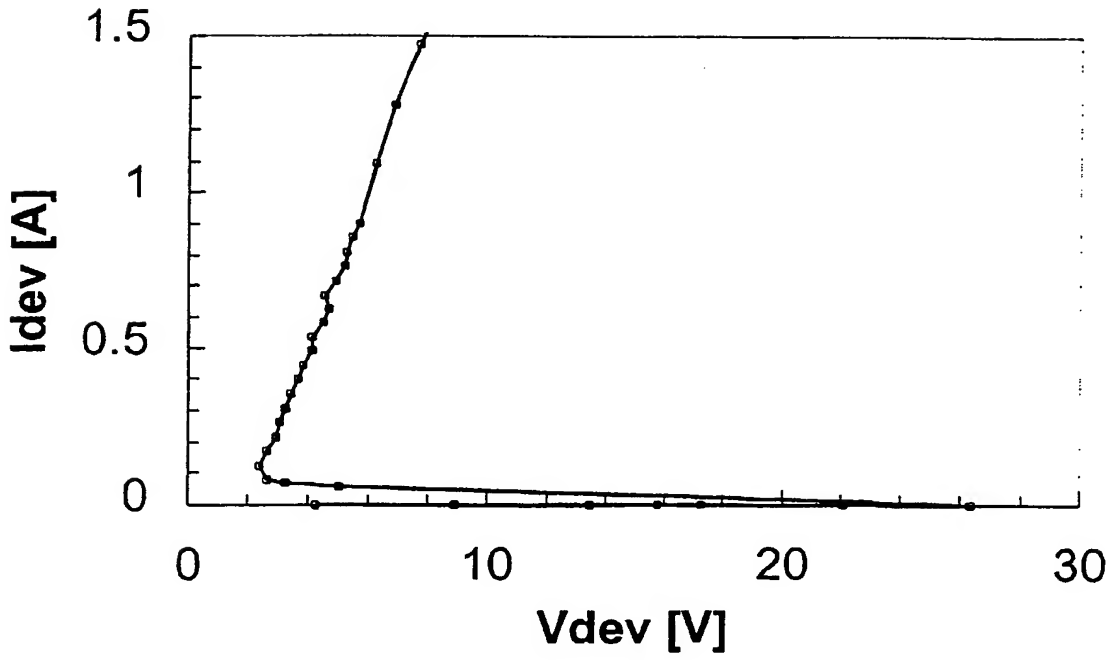
1.5
1
0.5
0
Idev [A]
0
10
20
30
Vdev [V]

FIG. 7

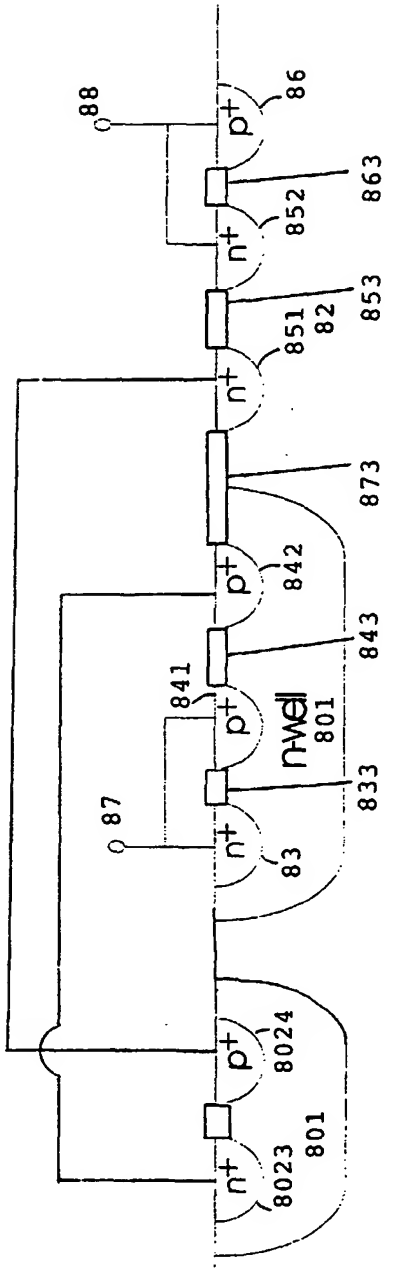
88
86
p+
863
852
n+
853
851
82
n+
873
842
p+
843
841
p+
n-well
801
833
87
n+
83
8024
p+
8023
n+
801

FIG. 8

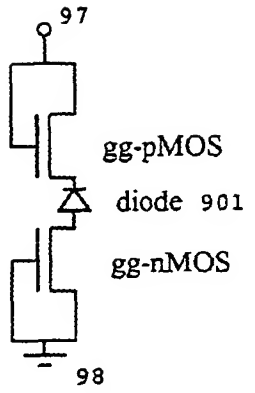

FIG. 9

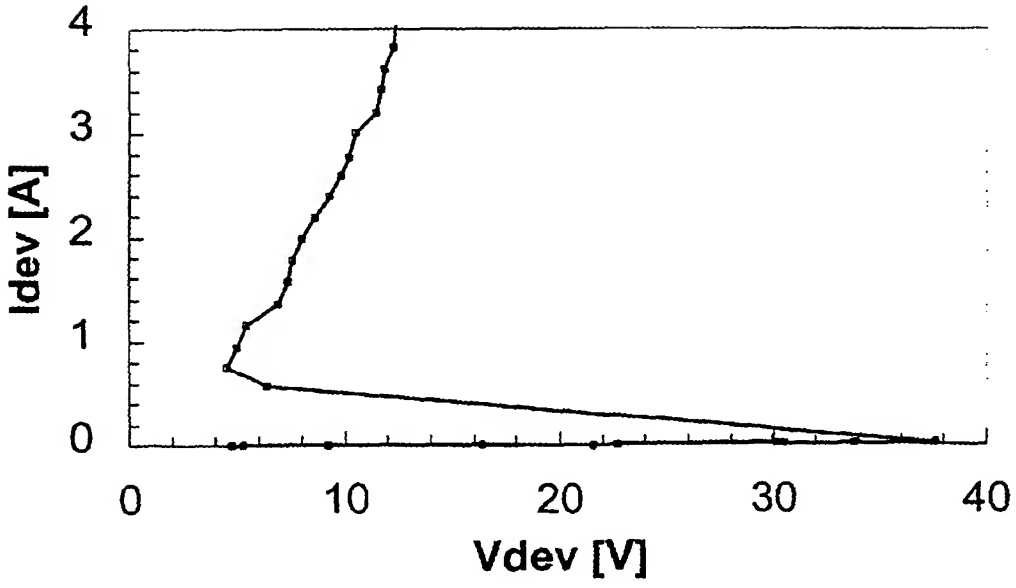

FIG. 10

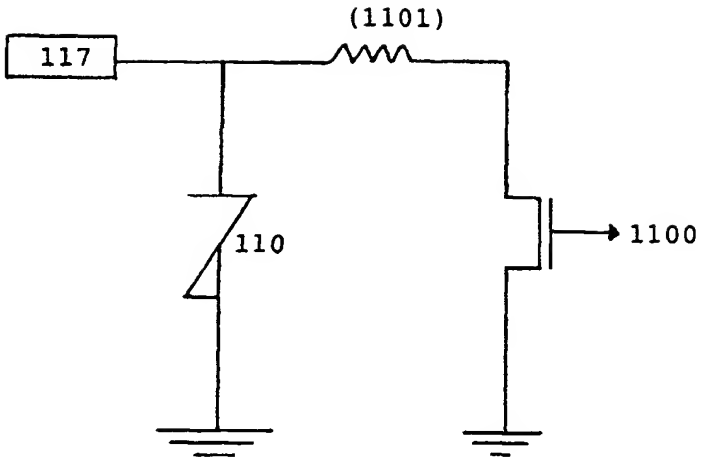

FIG. 11

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 87 0110

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 96 21247 A (PHILIP SHIOTA) 11 July 1996 (1996-07-11) * page 32, line 11 - page 33, line 29; figures 27A-29B *	1-21	H01L27/02 H01L29/87 H01L29/74
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H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 May 2000	Sinemus, M

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